

DHANALAKSHMI COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
EE6301 – DIGITAL LOGIC CIRCUITS
UNIT I – NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES

PART A

1. How can an OR gate be realized using a NAND gate? (M-13)
2. Define – Multiplexer (M-13)
3. What is meant by priority encoder? (M-12)
4. Distinguish between decoder and demultiplexer. (N-11)
5. State De-Morgan's theorem. (A-11)
6. Draw the truth table and logic circuit of a half adder. (A-10)
7. What is meant by decoder? (M-09)
8. What is meant by encoder? (M-10)
9. List out the applications of multiplexers. (M-09)
10. What is meant by demultiplexer? (M-08)

PART B

1. (i) Prove that $\bar{A}.B + A.\bar{B}$ is an exclusive OR operation and it equals to $\overline{(\bar{A}.B)} . \overline{(\bar{A}.B)} . B$
 (ii) Prove that for constructing XOR from NAND, four NAND gates are needed. (16) (M-13)
2. Simplify the given Boolean function, using K-map $F(w, x, y, z) = \Sigma (1,3,7,11,15)$, which has don't care conditions as $d(w, x, y, z) = \Sigma (0,2,5)$. (16) (M-13)
3. (i) Implement the Boolean function, $Y = AC + ABC + \bar{A}BC + AB + D$ with NAND-NAND logic. (6) (M-12)
 (ii) Simplify and implement the following SOP function using NOR gates:
 $F(x, y, z) = \Sigma (0,1,4,5,10,11,14,15)$ (10) (M-12)
4. (i) Implement the function, $F(x, y, z) = \Sigma (0,2,6,7)$ using multiplexer. (8) (M-12)
 (ii) Implement full subtractor using demultiplexer. (8) (M-12)
5. Obtain the simplified expression for the logic equation given by, $(A, B, C, D) = \Sigma m (0,8,11,12,15) + d(1,2,4,7,10,14)$, where d represents don't care condition. Write the simplified expression using logic gates. (16) (N-11)
6. Write short notes on the following:
 a) De-Morgan's theorem
 b) Comparator
 c) Binary to gray code converter
 d) Multiplexer (16) (N-11)
7. Reduce the following expressions using Boolean algebra: (16) (M-11)
 a) $\bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + \bar{x}yz + x\bar{y}z + xyz$
 b) $ab\bar{c} + a\bar{b}c + \bar{a}bc + abc$
 c) $\bar{p}\bar{q}r + \bar{p}q\bar{r} + \bar{p}qr + pq\bar{r} + p\bar{q}r$

8. (i) Reduce the given expression using K-map, $f = \bar{x}\bar{y}z + \bar{w}xz + wxy\bar{z} + wxz + \bar{w}xyz$.
(6) (M-11)
- (ii) Implement a full adder circuit with the following: (10) (M-11)
- a) Decoder
 - b) Multiplexer
9. Obtain the minimum SOP, using Quine Mcclusky's method and verify using K-map for the expression given by, $F(A, B, C, D) = \Sigma m (0, 2, 4, 8, 9, 10, 11, 12, 13)$. (16) (N-10)
10. (i) Simplify the expression given by, $F(w, x, y, z) = \Sigma m (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$, using K map. (8) (N-10)
- (ii) Design BCD to excess-3 code converter. (8) (N-10)

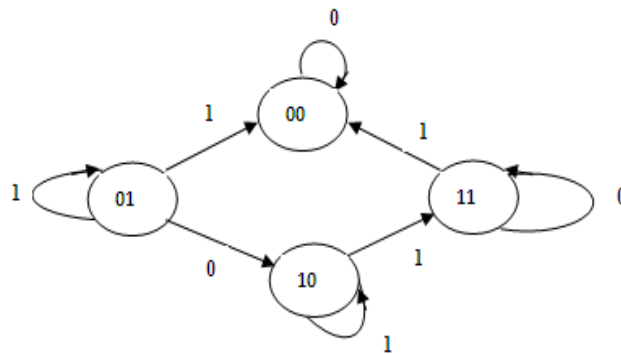
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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
EE6301 – DIGITAL LOGIC CIRCUITS
UNIT II – COMBINATIONAL CIRCUITS

PART A

1. Define – Flip Flop (M-13)
2. Define – Race Around Condition (N-12)
3. Compare combinational circuits with sequential circuits. (M-12)
4. What are the various classifications of sequential circuits? (N-11)
5. What is the operation of D flip-flop? (M-11)
6. What is meant by master-slave flip-flop? (M-10)
7. Write the excitation tables for a JK flip-flop. (N-09)
8. Compare synchronous counters with asynchronous counters. (M-10)
9. What is meant by edge-triggered flip-flop? (M-09)
10. What are the different types of flip-flop?

PART B

1. Design a synchronous sequential circuit using JK flip-flop for the state diagram given below. (16) (A/M-2010)



2. Design a BCD counter using T flip flop. (16) (AM/10)
3. Derive the state equation and draw the state diagram and the clocked sequential circuit for the state table given below. (16) (A/M-11)

Present State	Next State		Output	
	x=0	x=1	x=0	x=1
AB	AB	AB	Y	Y
00	00	01	0	0
01	11	01	0	0
10	10	00	0	0
11	10	11	0	0

4. Design a BCD counter using T flip flops, where flip flop inputs are TQ_1 , TQ_2 , TQ_4 and TQ_8 . (16) (A/M-11)
5. Design a counter with the sequence 0, 1, 3, 7, 6, 4, 0. (16) (N/D-10)
6. Design the counter for the following sequences which is consisting of 3 JK flip flops:
 - a) A1 0 0 0 0 1 1 0
 - b) A2 0 1 1 0 0 1 0
 - c) A3 0 1 0 1 1 0 0 (16) (N/D-10)
7. (i) Obtain a SR flip flop using NOR gates and explain its operation. (8) (M/J-12)
 (ii) Convert a SR flip flop into JK flip-flop. (8) (M/J-12)
8. Obtain the following for a sequential circuit with 2 D flip flops, A and B and input, X and output, Y which is specified below with the state and the output equations:

State equations: (i) $A(t+1) = AX + BX$ and (ii) $B(t+1) = A'X$

Output equation: $Y = (A + B) X'$

 - a) Draw the logic diagram of the circuit
 - b) Derive the state table
 - c) Draw the state diagram (16) (MJ/2012)
9. Design a 3-bit binary counter using a T flip flop. (16) (M/J-13)
10. Draw the state transition diagram of a sequence detector circuit that detects '1010' from input data stream using Moore model and Mealy model. (16) (N/D-11)
11. Design a counter using a JK flip flop for realizing the following sequence. (16) (N/D-11)

Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	1
1	1	1
1	1	0
1	0	0
0	0	0

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EE6301 – DIGITAL LOGIC CIRCUITS

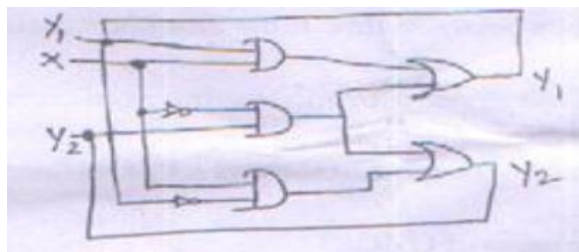
UNIT III – SYNCHRONOUS SEQUENTIAL CIRCUITS

PART A

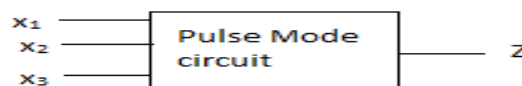
1. What is meant by race condition in asynchronous sequential circuit? (A-13)
2. What are called hazards? (N-12)
3. What are the assumptions made for fundamental mode circuit? (N-12)
4. Define – Flow Table in an asynchronous sequential circuit (A-12)
5. What are the steps to be followed in the designing of a asynchronous sequential circuit? (N-11)
6. Define – Static 0-Hazard, Static 1-Hazard and Dynamic Hazard (A-09)
7. What is meant by critical race? Why should it be avoided? (N-10)
8. What is meant by cycle? (A-12)
9. How does an essential hazard occur? (A-12)
10. What are the significances of state assignment?

PART B

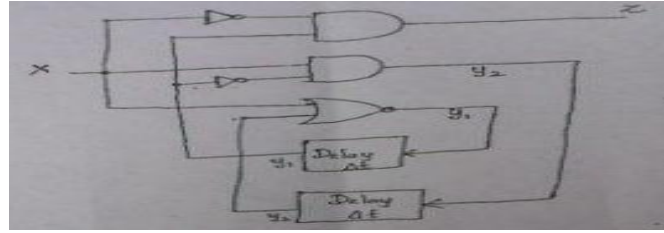
1. Consider the following asynchronous sequential circuit and draw the maps, transition table, and state table. (16) ((M-13))



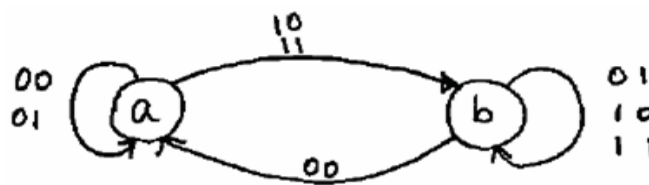
2. Illustrate the procedure of an asynchronous sequential circuit with an example. (16) (M-13)
3. Design a pulse mode circuit with inputs x_1 , x_2 , x_3 and output z as shown in figure below by considering the following necessary conditions:
 - a) the output should change from 0 to 1, only for the input sequence x_1 - x_2 - x_3 occurs, while $z=0$
 - b) the output z should remain in 1 until x_2 occurs
 - c) use only SR flip flops for the design
 (16) (M-13)



4. (i) Explain the steps used for analyzing an asynchronous sequential circuit. (8) (M-13)
(ii) Derive the flow table for the circuit given in the figure below. (8) (M-13)



5. (i) When does oscillation occur in an asynchronous sequential logic. (4) (N-11)
(ii) Draw and explain the state transition diagram for modulo-6 counter in an asynchronous sequential logic. (12) (N-11)
6. (i) Write the condition for stability in an asynchronous sequential logic. (4) (N-11)
(ii) Design an asynchronous sequential logic circuit for the state transition diagram shown in the figure below. (12) (N-11)



7. Design an asynchronous BCD counter. (16) (A-11)
8. Explain in detail, the steps involved in designing of an asynchronous sequential circuit with an example. (16) (A-11)
9. (i) Reduce the number of states in the following state table: (12) (A-11)

Present State	Next State		Output	
	X=0	X=1	X=0	X=1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	G	h	0	1
h	G	a	1	0

- (ii) Find the output sequence generated with input sequence 01110010011. (4) (A-11)
10. (i) List and explain the steps used for analysing an asynchronous sequential circuit. (8) (A-10)
(ii) What are called critical and non-critical races? Describe ways to obtain race free conditions. (8) (A-10)

UNIT IV**ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABLE
LOGIC DEVICES****PART-A**

1. Explain ROM. (N/D-12)
2. What are the various types of ROM? (M/J-11)
3. What is meant by programmable logic array? How does it differ from ROM? (M/J-10)
4. What is meant by CPLD? (M/J-13)
5. Define – Cache Memory (M/J-13)
6. Compare PROM with PLA. (N/D-09)
7. List out the classifications of a saturated bipolar logic families. (M/J-12)
8. Define – Fan-out (N/D-13)
9. Define – Noise Margin (M/J-12)
10. How are Schottky transistors formed? (N/D-12)

PART B

1. Explain in detail, the concept, working and the characteristics of TTL logic families. (8) (N/D-10)
2. What is meant by FPGA? Explain in detail, their operation and applications. (8) (N/D-10)
3. Explain in detail, the working of EPROM. Also list out their applications. (8) (A/M-11)
4. Explain in detail, the concept, operation and the characteristics of CMOS technology. (8) (A/M-11)
5. Explain in detail, the characteristics of various types of memories. (8) (A/M-11)
6. Design ROM for the function given by $F_1 = \Sigma(1, 2, 3)$; $F_2 = \Sigma(0, 2)$. (8) (A/M-11)
7. Explain in detail, the programmable logic devices. (8) (N/D-11)
8. Explain in detail, the characteristics of CMOS. (8) (N/D-11)
9. Explain in detail, the NOR gate using TTL logic with suitable diagrams. (8) (N/D-11)
10. A combinational logic circuit is defined by the functions given below.

$$F_1(a, b, c) = \Sigma(0, 1, 6, 7), F_2(a, b, c) = \Sigma(2, 3, 5, 7) \quad (16)$$
11. (i) Implement the circuit with a PAL having three inputs, three products terms and two outputs. (10) (M/J-12)
- (ii) Explain in detail, the concept and working of FPGA. (6) (M/J-12)

UNIT V – VHDL**PART A**

1. What is meant by verilog? (N/D-12)
2. What is meant by switch-level modeling? (M/J-10)
3. What are the called value sets in verilog? (N/D-11)
4. List out the various classifications of timing control. (M/J-11)
5. What are the various types of conditional statements? (M/J-12)
6. What are the various types of ports in verilog? (N/D-13)
7. What are the various modeling used in verilog? (M/J-09)
8. What is meant by structural gate-level modeling? (M/J-11)
9. What are called gate primitives? (N/D-12)
10. What are the various types of procedural assignments? (M/J-13)

PART B

1. Explain in detail, the structural VHDL description for a 2 to 4 decoder. (16) (N-13)
2. Write a VHDL program and explain in detail, the design procedure of 8 bit comparator. (16) (N-13)
3. Explain in detail, the RTL design using VHDL with an example. (16) (M-12)
4. Write the VHDL code for mod 6 counter. (16) (M-12)
5. Explain in detail, procedure for register transfer language. (16) (N-11)
6. (i) Construct a VHDL module for a JK flip flop. (8) (N-11)
- (ii) Express the expression for arithmetic and logic operations using RTL. (8) (N-11)
7. (i) Explain the VHDL code that implements an 8:1 multiplexer. (10) (N-12)
- (ii) Explain the different data types that supported in VHDL. (6) (N-12)
8. Explain in detail, the uses of packages in VHDL. (8) (N-12)
9. Explain in detail, the HDL program for a full adder and a 4-bit comparator. (16) (M-10)
10. Explain in detail, the HDL code for 8:1 multiplexer using behavioral model. (16) (N-10)